REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
D	Technical changes in 1.4 and table I. Editorial changes throughout.	91-10-30	M. A. Frye

CURRENT CAGE CODE 67268

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS OF SHEETS															
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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APPROVED BY
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DRAWING APPROVAL DATE
17 October 1984

REVISION LEVEL
D

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, HIGH-SPEED CMOS, FLIP-FLOPS, MONOLITHIC SILICON FILTER, MONOLITHIC SILICON

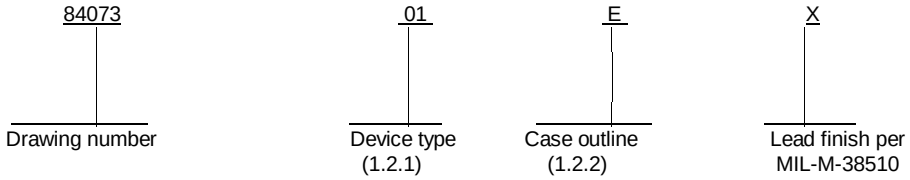
SIZE	CAGE CODE	
A	14933	84073

SHEET 1 OF 14

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54HC174	Hex D-type flip-flops with clear

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16-lead, .250" x .875"), dual-in-line package
F	F-5 (16-lead, .250" x .375"), flat package
2	C-2 (20-terminal, .350" x .350"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage	-0.5 V dc to V_{CC} +0.5 V dc
DC output voltage	-0.5 V dc to V_{CC} +0.5 V dc
Clamp diode current	±20 mA
DC output current (per pin	±25 mA
DC V_{CC} or GND current (per pin	±50 mA
Storage temperature range	-65° C to +150° C
Maximum power dissipation (P_D)	500 mW 2/
Lead temperature (soldering, 10 seconds)	+260° C
Thermal resistance, junction-to-case (Θ_{JC}):	
Cases E, F, and 2	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175° C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+2.0 V dc to +6.0 V dc
Input voltage range (V_{IN})	0.0 V to V_{CC}
Output voltge range (V_{OUT})	0.0 V to V_{CC}
Case operating temperature range (T_C)	-55° C to +125° C

1/ Unless otherwise specified all voltages are referenced to ground.
2/ For T_C = +100° C to +125° C, derate lineraly at 12 mW/° C.

Maximum operating frequency (f_{MAX}):

T_C = +25°C	
V_{CC} = 2.0 V dc	5.4 MHz
V_{CC} = 4.5 V dc	27 MHz
V_{CC} = 6.0 V dc	32 MHz
T_C = -55°C, +125°C	
V_{CC} = 2.0 V dc	3.6 MHz
V_{CC} = 4.5 V dc	18 MHz
V_{CC} = 6.0 V dc	21 MHz

Minimum removal time clear to clock (t_{REM}):

T_C = -55°C, +125°C	
V_{CC} = 2.0 V dc	100 ns
V_{CC} = 4.5 V dc	20 ns
V_{CC} = 6.0 V dc	17 ns
T_C = -55°C, +125°C	
V_{CC} = 2.0 V dc	150 ns
V_{CC} = 4.5 V dc	30 ns
V_{CC} = 6.0 V dc	26 ns

Minimum setup time, data to clock (t_S):

T_C = +25°C	
V_{CC} = 2.0 V dc	100 ns
V_{CC} = 4.5 V dc	20 ns
V_{CC} = 6.0 V dc	17 ns
T_C = -55°C, +125°C	
V_{CC} = 2.0 V dc	150 ns
V_{CC} = 4.5 V dc	30 ns
V_{CC} = 6.0 V dc	26 ns

Minimum hold time clock to data (t_h):

T_C = +25°C	
V_{CC} = 2.0 V dc	25 ns
V_{CC} = 4.5 V dc	5 ns
V_{CC} = 6.0 V dc	5 ns
T_C = -55°C, +125°C	
V_{CC} = 2.0 V dc	40 ns
V_{CC} = 4.5 V dc	8 ns
V_{CC} = 6.0 V dc	7 ns

Minimum pulse width, clock (t_{w1}):

T_C = +25°C	
V_{CC} = 2.0 V dc	90 ns
V_{CC} = 4.5 V dc	18 ns
V_{CC} = 6.0 V dc	15 ns
T_C = -55°C, +125°C	
V_{CC} = 2.0 V dc	135 ns
V_{CC} = 4.5 V dc	27 ns
V_{CC} = 6.0 V dc	23 ns

Minimum pulse width, clear (t_{w2}):

T_C = +25°C	
V_{CC} = 2.0 V dc	80 ns
V_{CC} = 4.5 V dc	16 ns
V_{CC} = 6.0 V dc	14 ns
T_C = -55°C, +125°C	
V_{CC} = 2.0 V dc	120 ns
V_{CC} = 4.5 V dc	24 ns
V_{CC} = 6.0 V dc	20 ns

Maximum input rise and fall time (t_r, t_f):

T_C = +25°C	
V_{CC} = 2.0 V dc	1000 ns
V_{CC} = 4.5 V dc	500 ns
V_{CC} = 6.0 V dc	400 ns
T_C = -55°C, +125°C	
V_{CC} = 2.0 V dc	1000 ns
V_{CC} = 4.5 V dc	500 ns
V_{CC} = 6.0 V dc	400 ns

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroup	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum, $\lvert I_O \rvert \le 20$ µA	$V_{CC} = 2.0$ V	1, 2, 3	1.9		V
			$V_{CC} = 4.5$ V		4.4		
			$V_{CC} = 6.0$ V		5.9		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum, $\lvert I_O \rvert \le 4.0$ mA	$V_{CC} = 4.5$ V		3.7		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum, $\lvert I_O \rvert \le 5.2$ mA	$V_{CC} = 6.0$ V		5.2		
Low level output voltage	V_{OL}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum, $\lvert I_O \rvert \le 20$ µA	$V_{CC} = 2.0$ V	1, 2, 3		0.1	V
			$V_{CC} = 4.5$ V			0.1	
			$V_{CC} = 6.0$ V			0.1	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum, $\lvert I_O \rvert \le 4.0$ mA	$V_{CC} = 4.5$ V			0.4	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum, $\lvert I_O \rvert \le 5.2$ mA	$V_{CC} = 6.0$ V			0.4	
High level input voltage 3/	V_{IH}		$V_{CC} = 2.0$ V	1, 2, 3	1.5		V
			$V_{CC} = 4.5$ V		3.15		
			$V_{CC} = 6.0$ V		4.2		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Low level input voltage 2/	V_{IL}		V_{CC} = 2.0 V	1, 2, 3		0.3	V
			V_{CC} = 4.5 V			0.9	
			V_{CC} = 6.0 V			1.2	
Input capacitance	C_{IN}	V_{IN} = 0 V, see 4.3.1c		4		10	pF
Quiescent current	I_{CC}	V_{CC} = 6.0, V_{IN} = V_{CC} or GND		1, 2, 3		160	µA
Input leakage current	I_{IN}	V_{CC} = 6.0 V_{IN} = V_{CC} or GND		1, 2, 3		±1	µA
Functional tests		See 4.3.1d		7			
Propagation delay time clock or clear to output 2/	t_{PHL}, t_{PLH}	T_C = +25°C C_L = 50 pF See figure 4	V_{CC} = 2.0 V	9		165	ns
			V_{CC} = 4.5 V			33	
			V_{CC} = 6.0 V			28	
		T_C = -55°C +125°C C_L = 50 pF See figure 4	V_{CC} = 2.0 V	10,11		250	ns
			V_{CC} = 4.5 V			50	
			V_{CC} = 6.0 V			43	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Transition delay time, output rise and fall 2/ 4/	t_{THL}, t_{TLH}	T_C = +25°C C_L = 50 pF See figure 4	V_{CC} = 2.0 V	9		75	ns
			V_{CC} = 4.5 V			15	
			V_{CC} = 6.0 V			13	
		T_C = -55°C +125°C C_L = 50 pF See figure 4	V_{CC} = 2.0 V	10,11		110	ns
			V_{CC} = 4.5 V			22	
			V_{CC} = 6.0 V			19	

1/ For a power supply of 5 V ±10%, the worst case output voltages (V_{OH} and V_{OL})occur for HC at 4.5 V. Thus, the 4.5 V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V, respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage current (I_{IN}, and I_{CC}) occur for CMOS at the higher voltage so the 6.0 V values should be used. Power dissipation capacitance (C_{PD}), typically 162 pF, determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}2 f+I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f+I_{CC}$.

2/ V_{IH} and V_{IL} tests are not required if applied as a forcing function for V_{OH} and V_{OL}.

3/ All testing at V_{CC} = 2.0 V and V_{CC} = 6.0 V shall be guaranteed, if not tested, to the specified parameters in table I.

4/ Transition times, if not tested, shall be guaranteed to the specified limits in table I.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full (case or ambient) operating temperature range.

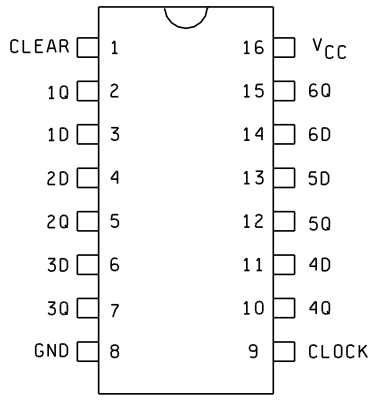
3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

CASES E AND F



CASE 2

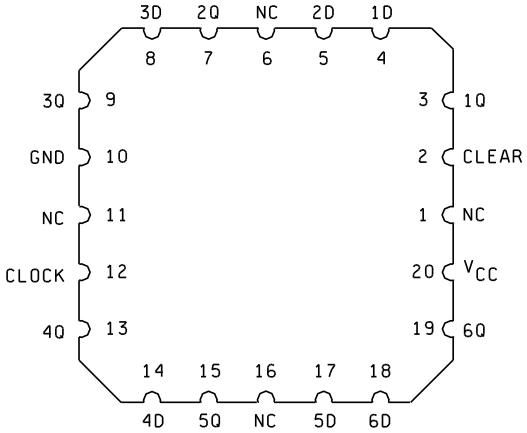


FIGURE 1. Terminal connections (top view).

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_O

H = High level (steady-state)
L = Low level (steady-state)
X = Don't care
↑ = Transition from low to high level
Q_O = The level of Q before the indicated input conditions were established.

FIGURE 2. Truth table.

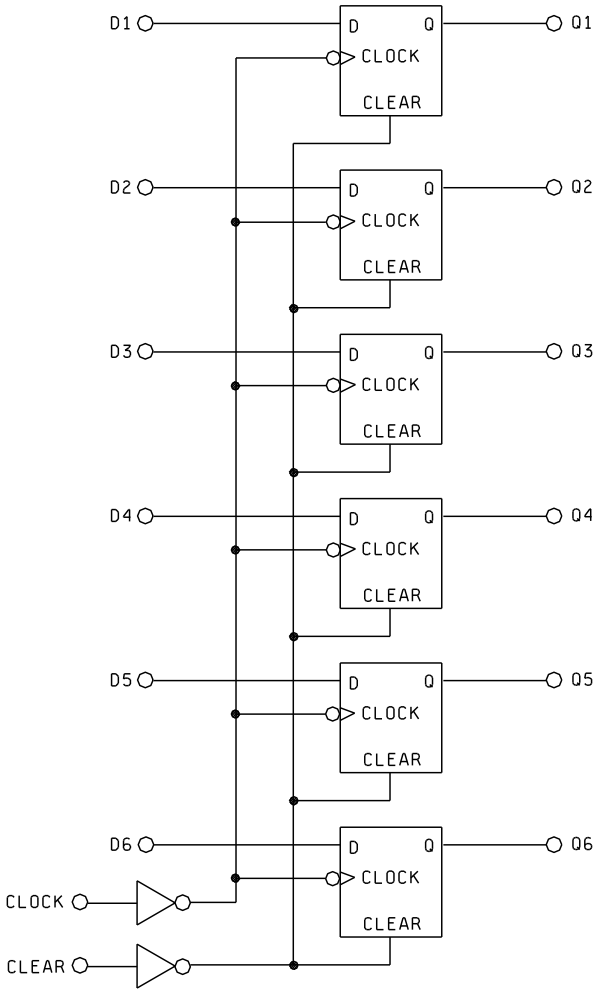
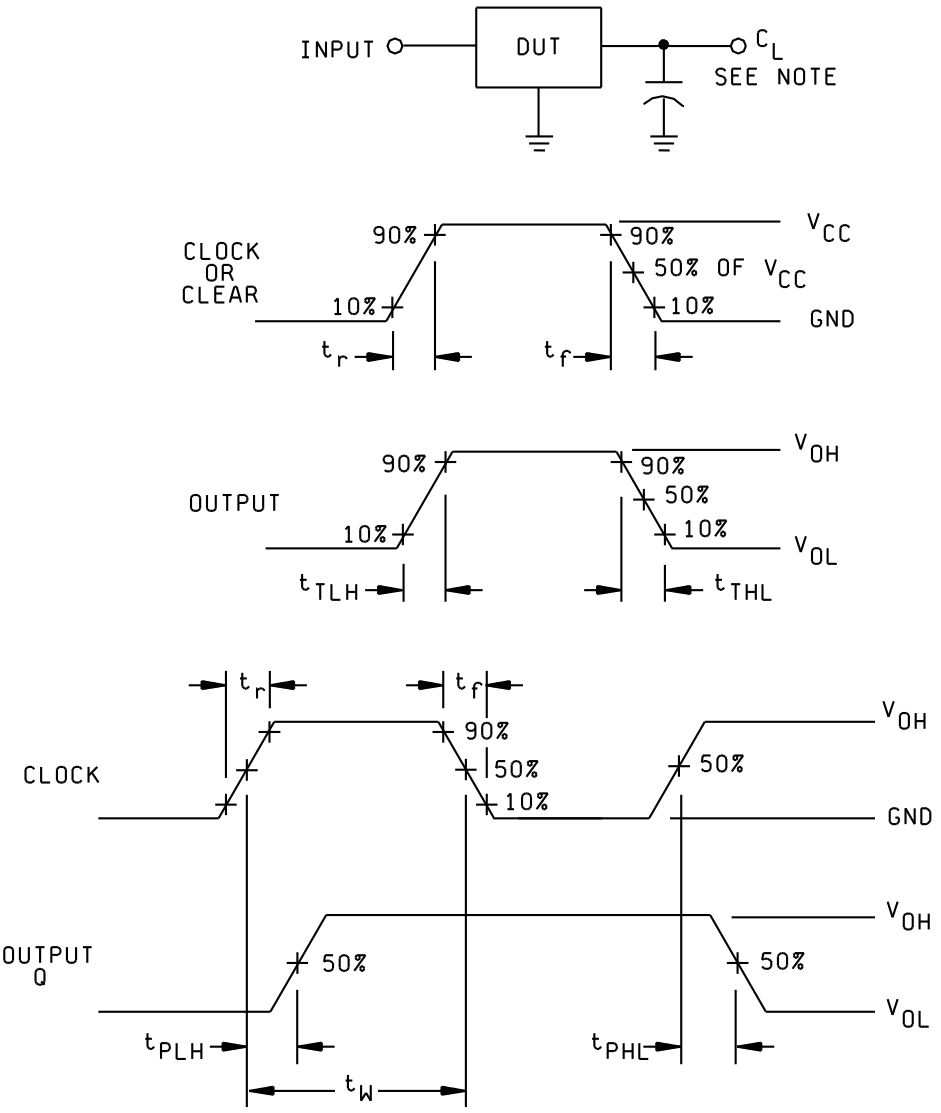
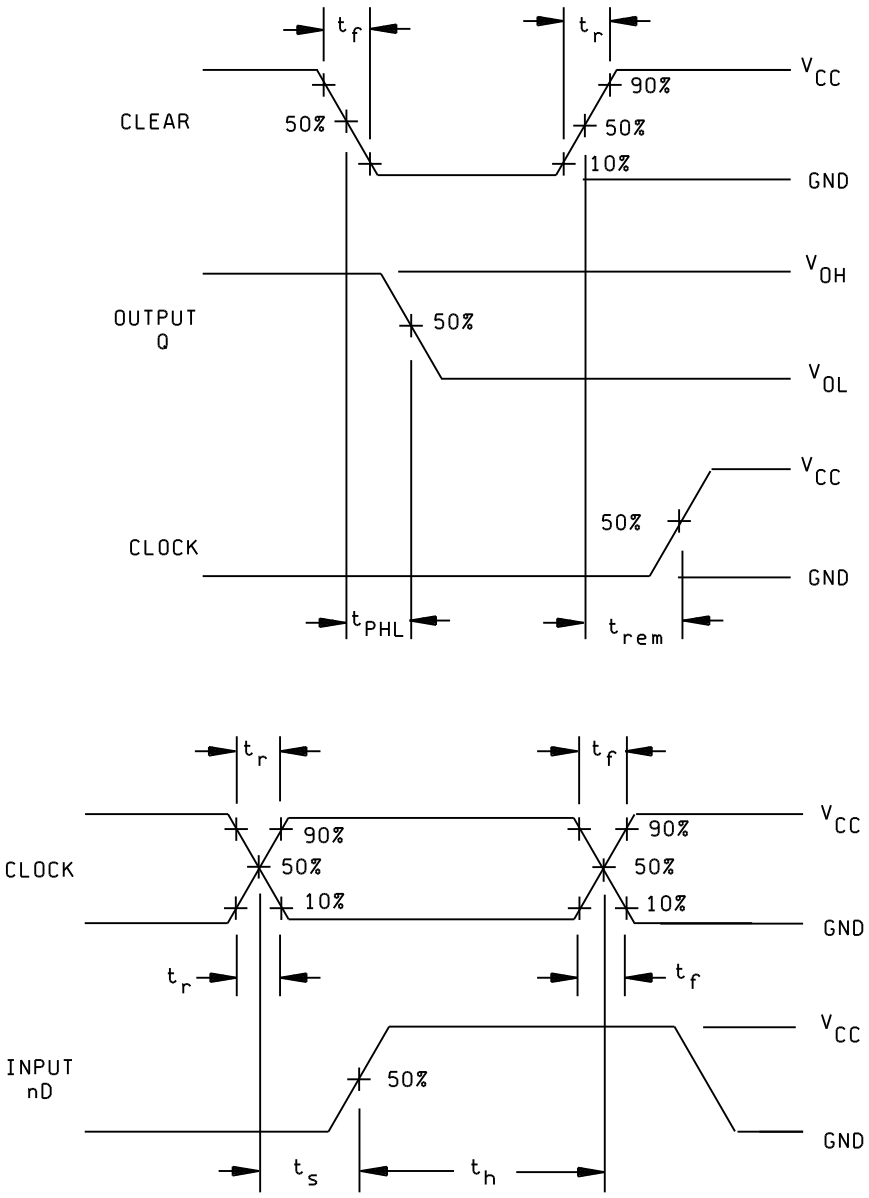


FIGURE 3. Logic diagram.



NOTE: C_L = 50 pF minimum, includes probe and jig capacitance.
$t_r \leq 6$ ns, $t_f \leq 6$ ns.

FIGURE 4. Switching waveforms and test circuit.



NOTE: $t_r \leq 6$ ns, $t_f \leq 6$ ns.
t_r is measured from the 10% point to the 90% point.
t_r is measured from the 90% point to the 10% point.

FIGURE 4. Switching waveforms and test circuit - Continued.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

*PDA applies to subgroup 1.
**Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Test all applicable pins on five devices with zero failures.

d. Subgroup 7 tests shall verify the truth table as specified on figure 2.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the device specified in this drawing will be replaced by the microcircuit identified as PIN M38510/65307BXX.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 91-10-30

Approved sources of supply for SMD 84073 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/	Replacement military specification PIN
8407301EX 2/	04713 01295 27014 34371	54HC174/BEAJC SNJ54HC174J MM54CH174J/883B CD54HC174F/3A	M38510/65307BEX
8407301FX	01295	SNJ54HC174W	M38510/65307BFX
84073012X	04713 01295 27014	54HC174M/B2AJC SNJ54HC174FK MM54HC174E/883	M38510/65307B2X

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
2/ Inactive for new design. Use 38510/63507BEX.

Vendor CAGE number	Vendor name and address
04713	Motorola, Incorporated 7402 South Price Road Tempe, AZ 85283
01295	Texas Instruments, Incorporated P.O. Box 60448 Midland, TX 79711-0448
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090 Point of contact: 333 Western Ave. South Portland, ME 04106
34371	Harris Semiconductor P.O. Box 883 Melbourne, FL 32901